

Terminator 3 ASIC

Third-Generation 10Gb Ethernet Unified Wire Engine for iSCSI, RDMA and TCP/IP Applications

Highlights

- High-performance server adapter, TCP/IP offload, iSCSI and RDMA
- Integrated traffic manager, QoS and virtualization capabilities
- Integrated PCI-X 2.0 266MHz and PCI-Express x8 host bus interfaces
- Integrated two 10Gb full-duplex Ethernet and two 100Mb/1Gb Ethernet MACs
- Support for additional external MACs
- Extensive system management interfaces including I²C, SMBus and IPMI
- Line-rate 10Gb full-duplex performance
- Powerful per-connection, per-server, and per-interface configuration and control
- Scalable to one million simultaneous connections

Benefits

- 'Unified Wire' interconnect solution for server networking, storage networking and clustering on a single platform
- Transforms Ethernet into a reliable, traffic-managed fabric
- Enables 2-port 10GbE and 2-port 1GbE solutions
- Supports up to 16-port 1GbE configuration
- Reduces host CPU utilization by up to 90% compared to server NICs
- Programmable, upgradeable solution
- Robust, stable and proven third-generation architecture reduces design risk

Applications

- Networking
- Storage
- High performance computing clusters
- Security and firewalls
- Virtualization
- Network traffic management
- Media streaming
- Application servers

THE TERMINATOR 3 ASIC from Chelsio Communications is a scalable high performance 10Gb Ethernet unified wire engine, enabling simultaneous support of iSCSI, RDMA and TCP/IP sockets applications. A third-generation design, it builds upon Chelsio's robust and field-proven Terminator 2 engine which has been widely deployed in server, storage and clustering interconnect applications.

Terminator 3 uses an ultra-low latency, high-bandwidth, programmable data-flow processor core, in conjunction with high bandwidth, fully ECC protected external memory interfaces, to provide no-compromise wire speed iSCSI, RDMA and TCP/IP performance. The highly programmable and flexible processor loads instructions at boot time, facilitating field upgrades.



Third-Generation Protocol Offload Engine

Chelsio's performance leading Terminator architecture processes all connections in one data-flow pipeline to deliver line-rate 10Gb throughput for a single connection, up to thousands of connections. In contrast, competing multi-RISC offload engines require multiple connections to distribute processing among the embedded processors, exhibit poor scaling, and are ultimately limited by the performance of each processor and by memory contention.

Terminator 3 benefits from significant design reuse of Chelsio's proven first- and second-generation Terminator engines, while adding numerous improvements, and a number of key new features, which include:

- Support for IETF RDDP and RDMAC iWARP
- Integrated Traffic Manager with QoS support
- Powerful traffic steering and virtualization capabilities
- Native PCI Express and PCI-X 2.0 host bus interfaces
- Integrated two 10GbE ports and two 1GbE ports
- Extensive system management interfaces

In addition, Terminator 3 reduces system costs by using commodity DDR2 memory, and integrating multiple Ethernet MACs.

Fully Featured Server Adapter

The Terminator 3 (T3) ASIC is a full-featured, stateless-offload server adapter engine. T3 based adapters offer best-of-class performance and features, including IP/UDP/TCP checksum and large send offload, rate control, virtualization, and rule-based traffic steering and filtering.

Complete and Flexible TCP/IP Offload

In addition to instructions loadable at boot-time, the T3 ASIC protocol offload configuration is fully programmable through register access. According to the host's policy, T3 can offload TCP processing per-connection, per-server, per-interface, and globally. It can also simultaneously tunnel traffic from non-offloaded connections to the host processor for the native software stack to process. T3 also provides a flexible zero-copy on receive capability for regular TCP applications, requiring no changes to the sender stack, or receiving application. With zero copy, line rate performance can be achieved at minimal CPU utilization.

iSCSI, RDMA and Upper Layer Protocols

The T3 ASIC offloads the expensive byte touching iSCSI operations and payload placement to greatly improve performance for IP SAN applications while maintaining flexibility. T3 also introduces a standards compliant, low latency, high bandwidth iWARP RDMA/RDDP implementation for cluster-interconnect applications. T3's architecture features an ideal work division between an embedded microprocessor and hardware-based state machines, to deliver optimum performance and flexibility for upper layer protocol support.

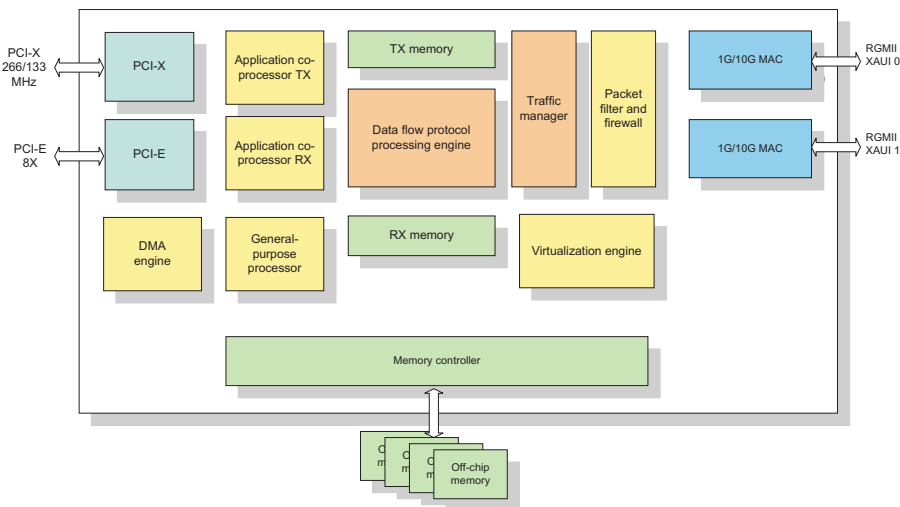
Robust, Proven Solution

Subjected to thousands of hours of compatibility testing, over two years of stress testing by several OEMs, and production deployments in servers, storage systems and cluster computing, Chelsio's robust, stable protocol offload technology delivers proven performance in all environments and network architectures.

Software Drivers and Design Kits

Chelsio offers a full suite of protocol software and drivers for Linux and Windows for its line of T3-based host bus adapters. The software supports operation in both protocol-offload and non-offload modes. Chelsio's software design kit includes reference-implementation source code, a programmer's guide, and porting guides for NIC, TOE, iSCSI and RDMA. Chelsio's hardware design kit includes reference design schematics, BOM, layout guidelines, ASIC data-book, BSDL file and I/O models for both 1Gb and 10Gb designs.

Block Diagram



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Specifications

Host Interface

- PCI Express x8
- PCI-X 2.0 266MHz downward compatible
- MSI-X, MSI and support for legacy pin interrupts

Network Interfaces

- Two RGMII interfaces for 1Gb operation
- Two XAUI interfaces for 10Gb operation
- IEEE 802.3ap 10GBASE-CX4 compliant

Ethernet

- IEEE 802.3ae (10GbE) and 802.3z (1GbE) compliant
- IEEE 802.1p Priority and 802.1Q VLAN tagging
- IEEE 802.3x flow control
- IEEE 802.3ad load-balancing and failover
- Ether II and 802.3 encapsulated frames
- Multiple MAC addresses per interface
- Jumbo Frames up to 9.6Kbytes

Stateless Offloads

- TCP checksum offload for IPv4 & IPv6
- TCP Segmentation Offload (TSO) for IPv4 & IPv6
- UDP checksum offload for IPv4 & IPv6
- UDP checksum over fragment offload
- Receive Side Scaling and packet steering
- Line rate packet filtering and attack protection

TCP/IP Full Offload

- Full TCP implementation including exceptions
- High performance even in presence of packet loss
- Extensive RFC compliance, fully featured stack
- Direct Data Placement (DDP)
- 1M simultaneous connections capacity

Integrated Traffic Manager

- Multiple transmit and receive queues with QoS
- Simultaneous low latency & high bandwidth
- Per-connection and per-class rate control
- Packet loss avoidance

Virtualization and Firewall

- Rule-based packet steering and filtering capability
- Tens of thousands of steering and filtering rules

iSCSI Acceleration

- Full iSCSI initiator and target mode stack
- Header & Data Digest (CRC) generation & checking
- PDU recovery
- Direct Data Placement (DDP)

High Performance RDMA

- Ultra-low latency, line rate bandwidth
- 64K simultaneous connections
- IEFT RDDP and RDMAC iWARP compliance
- APIs: RNIC-PI, kDAPL and OpenFabrics

Physical and Environmental

- 37mm x 37mm FCBGA package
- 0.13µm CMOS process technology
- Operating Temperature: 0 to 55 °C
- Operating Humidity: 5 to 95%
- 1.0, 1.2, 1.8, 2.5, 3.3 Volt operation
- Typical power consumption: 10W